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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/586,217 | 07/14/2006 | Johannes Dingenus Dingemanse | NL04 0062 US1 | 2771 |

65913 7590 10/10/2008

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| EXAMINER | |
|---|---|
| KERVEROS, JAMES C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2117 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 10/10/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/586,217 | DINGEMANSE, JOHANNES DINGENUS | |
| | Examiner | Art Unit | |
| | JAMES C. KERVEROS | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This is a non-Final Office Action in response to the AMENDMENT filed 8/29/2008.

The present US Application 10586217, filed 07/14/2006, is a national stage entry of PCT/IB05/50152 international, filed 01/13/2005.

Claims 1-10 are presently under examination and pending.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file, for the (EPO) Patent Application No. 04100143.9, filed 01/19/2004.

The Replacement Drawings received on 8/29/2008 are acceptable

Therefore, the rejection to the drawings has been withdrawn.

### *Response to Arguments*

Applicant's arguments with respect to the rejection of Claims 1-10 under 35 U.S.C. 102(b) as being anticipated by Wang et al. (US 20020184560) have been considered but are moot in view of the new ground(s) of rejection, as set forth in the present Office Action, next.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 3 and 6 recite the limitation, "wherein a particular test pattern in the selected set that has the properties that", which renders the claims indefinite, because it is not clear how the properties in the particular test pattern perform the particular function following the phrase "that". It is unclear whether the limitations following the phrase "that" are part of the claimed invention.

Also, the following limitations are replete with indefinite expressions, as shown by the quotations:

the response to the particular test pattern captured by a timing sensitive flip-flop cell in a first clock domain "is used" to detect a fault,

the timing sensitive flip-flop cell receives data dependent on data from a source flip-flop cell "that belongs to" a second clock domain different from the first clock domain,

the combination of selectively enabled domain clock signals "associated with" the particular test pattern comprises the clocks of both the first and second domain,

"also has the further property that the data value" in the source flip-flop cell is identical to a response value captured by the source flip-flop cell for the particular test pattern.

The claims are generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign

document and are replete with grammatical and idiomatic errors. Applicant should amend all the claims accordingly to comply with the U.S. practice, by mainly avoiding long narrative statements, thus making the claims incomprehensible.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Nadeau-Dostie et al. (U.S. Patent No. 6,442,722) issued: August 27, 2002.

Regarding independent Claims 1-10, Nadeau-Dostie discloses a method and apparatus of testing a circuit having two or more clock domains at respective domain test clock rates and under control of a main test clock signal, the circuit having core logic, a plurality of scannable memory elements, each having a clock input, an input connected to an output of the core logic and/or an output connected to an input to the core logic, and configurable in scan mode in which the memory elements are connected to define one or more scan chains in each domain and in normal mode in which the memory elements are connected to the core logic in normal operational mode, as described in the Abstract and a first embodiment of Figs. 1-4, comprising:

a test controller (a Built-In Self-Test (BIST) controller 50) arranged to switch the circuit under test (integrated circuit, IC 10), having core logic 12 partitioned into two clock domains including a low speed domain 14 and a high speed domain 16, to a test mode by supplying a scan enable signal SE to scan chains 24 and 32 formed by two scannable memory elements (20, 22) and (28, 30), respectively.

The test controller BIST 50 supplies successive test input patterns generated by a Pseudo Random Pattern Generator (PRPG) coupled to an output bus 54 connected to the input of each scan chain in the circuit (SI). The test controller 50 also includes a Multiple Input Signature Analyzer (MISR) coupled to input bus 56 connected to the output of each of the scan chains (SO). The controller 50 delivers scan test vectors to the various scan chains along output bus 54 and receives responses from the scan chains along input bus 56, as shown in Figs. 1-4.

A test pattern selector corresponding to an (auxiliary test controller 52), which controls the configuration of the memory elements in its associated clock domain and applies an appropriate clock signal to the memory elements in response to the configuration control signal provided by the main test controller. The auxiliary test controller uses the main test clock for shifting all but a predetermined number of bits of the test stimulus (selected set) into the high speed scan chain 32 and for shifting captured data out of the scan chain and uses a predetermined domain clock signal to perform a capture sequence which includes launching the last bit and performing a capture operation, Fig. 4, which shows that the capture clock signal is active throughout

all of the scan-in and scan-out cycles and is inactive for two domain test clock cycles which effect the launch of the test vector and the capture in the high speed domain.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/
Primary Examiner, Art Unit 2117

Date: 9 October 2008
Office Action: Non-Final Rejection

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